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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/067,554	02/04/2002	Hae-Seung Lee	RPD00085	9601

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EXAMINER	
SOHN, SEUNG C	

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 02/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/067,554	LEE, HAE-SEUNG	
	Examin r	Art Unit	
	Seung C. Sohn	2878	

-- Th MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-40 are rejected under 35 U.S.C. 102(e) as being anticipated by Kozlowski et al. (Patent No. US 6,532,040).

Referring to claims 1, 13 and 25, Kozlowski et al. shows in Fig. 3 the following elements of Applicant's claim:

a) a plurality of pixels (dotted box) each having an output (Vn), each pixel including: a first circuit that produces a signal proportional to incident light intensity, said first circuit being connected to supply said proportional signal to said pixel output, a select node (ROW SELECT) connected to receive a select signal for selecting said pixel from said plurality of pixels, and a reset transistor (M3) for resetting said pixel (Col. 7, lines 1-34);

b) an amplifier (50) having: a first input for receiving said outputs (Vn) of said pixels, and an output coupled to said reset transistors to provide a negative feedback signal to a selected pixel (Col. 8, lines 23-42); and

c) a reset reference voltage source (REF) connected to apply a reset reference voltage signal to said amplifier to provide a voltage reference for controlling reset of said pixels (Col. 8, lines 43-60).

Referring to claims 2, 14 and 26, Kozlowski et al. shows in Fig. 3 that said amplifier (50) further includes a second input (+ input) receiving said reset reference voltage signal (REF).

Referring to claims 3, 15 and 27, Kozlowski et al. shows in Fig. 3 that said reset transistor (M3) includes a gate and first and second terminals, said first terminal connected to receive said negative feedback signal to adjust said second terminal's voltage to a selected reset voltage (Col. 8, lines 23-42).

Referring to claims 4, 16 and 28, Kozlowski et al. discloses that said reset reference voltage source signal (REF) is selected to control said voltage at said second reset transistor terminal to be about VT-deltaV below a reset voltage applied at said gate terminal of said reset transistor, where VT is a threshold voltage that is characteristic of said reset transistor, and deltaV is selected to maintain said reset transistor in a subthreshold region of operation during a steady state phase of pixel reset (Col. 7, lines 1-34).

Referring to claims 5, 17 and 29, Kozlowski et al. disclosesthat said selected deltaV is greater than about one hundred millivolts (Col. 8, lines 15-22).

Referring to claims 6, 18 and 30, Kozlowski et al. shows in Fig. 3 that said select node (ROW SELECT) of each said pixel comprises a terminal of a row select transistor (M2) that is coupled to said first input of said amplifier (50).

Referring to claims 7, 19 and 31, Kozlowski et al. shows in Fig. 3 that each said pixel further comprises a source follower transistor (M1) coupled between said second terminal of said reset transistor (M3) and a terminal of said row select transistor (M2).

Referring to claims 8, 11, 20, 23, 32 and 35, Kozlowski et al. shows in Fig. 3 that said first circuit comprises a photocircuit.

Referring to claims 9, 21 and 33, Kozlowski et al. shows in Fig. 3 that said amplifier comprises a differential amplifier including a first differential amplifier input transistor connected to receive said first amplifier input and a second differential amplifier input transistor connected to receive said second amplifier input, said first and second differential amplifier input transistors connected to provide a signal to a current mirror circuit that is connected to deliver said negative feedback signal to said reset transistor first terminal.

Referring to claims 10, 12, 22, 24, 34 and 36, Kozlowski et al. shows in Fig. 3 that said photocircuit includes a photodiode (12) and a capacitance (Cfb).

Referring to claims 37 and 38, Kozlowski et al. shows in Fig. 3 that said image sensor comprises a CMOS-compatible image sensor (Col. 3, lines 54-56).

Referring to claims 39 and 40, Kozlowski et al. shows in Fig. 3 that said pixels comprise active pixels (Col. 1, lines 11-13).

Response to Arguments

3. Applicant's arguments filed on November 7, 2003 have been fully considered but they are not persuasive. Kozlowski et al. shows in Fig. 3 an amplifier (50) having a first

input for receiving said outputs (Vn) of said pixels and an output coupled to said reset transistors (through M4) to provide a negative feedback signal to a selected pixel (Col. 8, lines 23-42). It is not necessary for coupling to be directly connected. Also, the invention as claimed does not claim whether the reset transistor is active or not when providing a negative feedback signal. It should be noted that it is the claims that define the claimed invention, and it is the claims, not the specification, that are anticipated or unpatentable.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seung C. Sohn whose telephone number is (571) 272-

2446. The examiner can normally be reached on Monday through Friday from 8:30 am to 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached on (571) 272-2444. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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SHANH X. LUU
PATENT EXAMINER